REMARKS

We are in receipt of the Office Action dated February 18, 2003, and the following remarks are made in light thereof.

Claims 1-27 and 64-79 are pending in the application, with claims 28-63 having been withdrawn and cancelled pursuant to a restriction requirement.

In the Office Action, claims 1, 3, 4, 6, 8, 9, 10, 12, 13, 15, 17, 18, 19, 21, 22, 24, 26, 27, and 64-79 are rejected on the basis of obviousness. Claims 2, 5, 7, 11, 14, 16, 20, 23, and 25 are objected to as being dependent upon a rejected base claim, but are held to be otherwise allowable if rewritten in independent form, which Applicant gratefully acknowledges.

The present invention relates to a semiconductor device. In particular, the semiconductor device includes the structural features shown in Figs. 6A-6C (top view) or in Figs. 8A-8C (cross-sectional view). There are seven independent claims pending in this application (i.e., claims 1, 10, 19, 64, 68, 72, and 76), with claim 64 being the broadest claim. Claim 64 recites a semiconductor device which requires:

a semiconductor layer (104 or 105) that is formed over a substrate (101), with the semiconductor layer comprising a pair of impurity regions and a channel region interposed therebetween;

a gate electrode (128 or 129) that is formed over said channel region with a gate insulating film (120) interposed therebetween, said gate electrode comprising a first conductive layer; and

a gate wiring (147) that is in contact with the gate electrode, the gate wiring comprising a second conductive layer;

wherein the gate wiring is provided outside the channel region (as shown in Figs. 6C or 8C).

Independent claims 1, 10 and 19 also recite that the gate electrodes are in electrical contact through connectors with gate wiring and the connectors are provided outside the channel forming region, which is also supported in Fig. 6C or Fig. 8C.

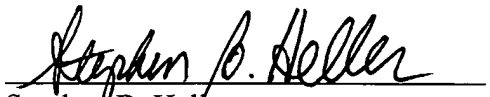
Each of the independent claims is rejected for being obvious over Yamanaka et al. 6,504,215, Kobayashi et al. 6,146,930 and Seo 6,323,068, in various combinations.

None of the prior art references relied upon by the Examiner teach or suggest a gate wiring that is provided outside the channel region, as is recited in claims 64, 68, 72 and 76, or connectors which are provided outside the channel forming region, as recited in claims 1, 10 and 19. Accordingly, Applicant submits that these claims are not obvious in view of the cited references.

In the foregoing Amendment, Applicant is also making some simple changes to the description of the figures of the drawings to identify Figs. 8A-8C and 9A-9C as cross-sectional views rather than top views.

In view of the foregoing, Applicant respectfully submits that the present application is in condition for allowance, and an early Office Action in this regard is earnestly solicited.

Respectfully submitted,



Stephen B. Heller
Registration No.: 30,181

COOK, ALEX, McFARRON, MANZO
CUMMINGS & MEHLER, LTD.
200 West Adams Street, Suite 2850
Chicago, Illinois 60606
(312)236-8500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 8, line 10 of the specification has been amended as follows:

Fig. 8A to 8C are ~~top~~ cross-sectional views of fabrication steps for a drive circuit TFT;

Page 8, line 11 of the specification has been amended as follows:

Fig. 9A to 9C are ~~top~~ cross-sectional views of fabrication steps for a pixel TFT;